

LABORATORY V

BAE 5413

SPRING 2007

TITLE: DIGITAL SIGNALS - INTERFACING TECHNIQUES

OBJECTIVE: To survey techniques used in interfacing digital signals to computer parallel interfaces and understand the nature of logic signals.

REFERENCES: Texas Instruments TTL Data Book, or Motorola Schottky TTL Data.

PROCEDURE:

Basic Logic Gates - Truth Tables: Install a 7400, 7404, 7402 in your breadboard. Connect one at a time to power, (pin 14 = 5V, pin 7 = GND). Select a gate on the chip and install an LED on the output of the gate as shown below in Figure 1. This circuit will serve as an indicator of the logic level being produced by the gate. Current through the LED should be limited to no more than 20 ma by the resistor. Please check and report this calculation for a nominal 5V logic output. Determine and report the size of resistor necessary. Develop and report a truth table for the gate by connecting each input to +5V, 0V, or Unconnected. All combinations of inputs should be tested. The truth table should list the gate output for all combinations of inputs. Repeat the process for each of the gate types. For TTL, by examining the output, what state is an unconnected input assumed to be?

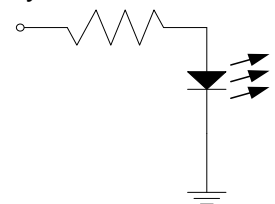


Figure 1

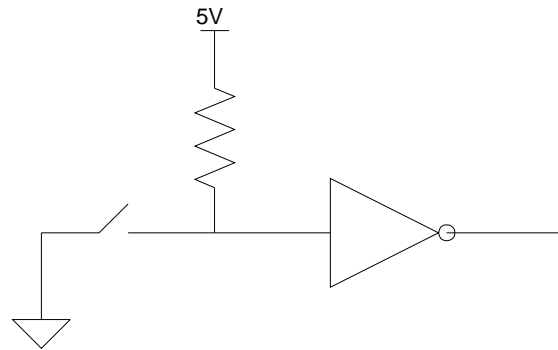
TTL Signal Levels - Determine the **input** voltage ranges that result in TRUE (Nominally +5V) and FALSE (Nominally 0V) outputs for a gate on the 7404. To do this use an LED to indicate output. Use a variable supply to provide the input voltage. Vary the input voltage from 0 to 5 V while observing the output. Repeat the experiment for 5 to 0 V. Record your results, and compare them to specifications for the chip. Determine and record the output drive current available from 74LS logic. Explain the sign on the currents. Does this type of logic have higher drive capability when driving a load at a low level or at a high level?

FLICKER THRESHOLD - Use the function generator to provide a TTL clock input to the above 7404 circuit. Determine the frequency at which your eye can no longer detect flicker in the LED (use a red LED). Test while looking directly into the LED and also looking to the side. Report these frequencies. Provide comment and reference to educated speculation on the reason for this phenomena which may also be known as critical fusion frequency.

OPEN COLLECTOR OUTPUTS - Develop and report a truth table for a 74LSS05 gate by connecting each input to +5V, 0V, or Unconnected. All combinations of inputs should be tried. Repeat the test with a 10 K Pull-up resistor connected from the gate to 5V. The output should still be measured at the gate output. Draw conclusions and report regarding the need for pull-up resistors on open collector gates.

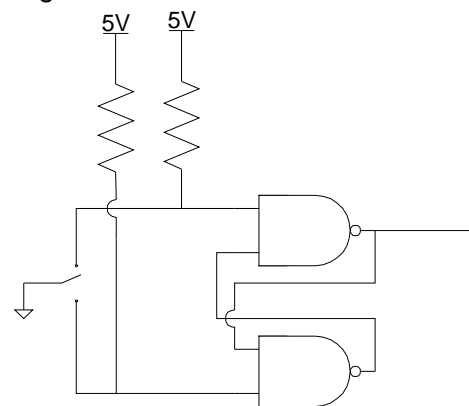
SWITCH INPUTS - Connect a switch and resistor as shown in figure 2. Use one of the switches on the breadboard. Confirm that the output will set the input levels on a TTL gate with a 10K resistor. Report how this resistor should be sized. Use a digital sampling oscilloscope to observe the output of the circuit. Set the scope to allow observation of 30kHz signals and to trigger a single trace on the initial change of state. Determine and report the number of transitions of the output for each switch transition. Record your results.

Figure 2



SWITCH DEBOUNCING - Connect the circuit as shown in Figure 3. Use the DPST switch in the breadboard to construct the circuit. Use a digital sampling scope to capture the output of this circuit. Sketch and compare the output of the circuit above with this circuit.(sketch both traces).

Figure 3



SIMPLE CLOCK - Using the handout on the 555 timer, construct an astable timer circuit like the one in the reference handout (NE_SA555X.pdf). Use R_a and R_b values of 10K and a capacitance of 0.1 μF . Power the circuit and examine the output. What kind of output do you get and is it as expected? Report the error in the period of the output compared to the calculated period?

ONE SHOT - Create a mono-stable pulse (one-shot) using the 555 timer. Use the circuit diagram in the second figure of the reference handout (NE_SA555X.pdf). Use a capacitor of approximately 10 μF and a 10K resistor. Use a switch to trigger the timer. Note that the trigger must be maintained high and triggers when dropped momentarily below $1/3 V_{cc}$. Report and compare the measured time delay and expected time delay.

BI-POLAR JUNCTION TRANSISTOR OUTPUT

– Breadboard the following transistor circuit which is configured to drive a load (R_2). Critical specifications on the transistor are its current gain, β , and maximum collector-base, and base-emitter voltage. The transistor's current gain may be used to calculate the collector current given the base current in a linear operating mode. Check the following circuit and determine the current gain experimentally. Note that the 1K resistor on the base is included to limit the base current to a level that does not damage the transistor.

