Advanced Agricultural Electronics Networks Development

Lecture No. 9, Load switching

BAE 5030-352

Spring 2010

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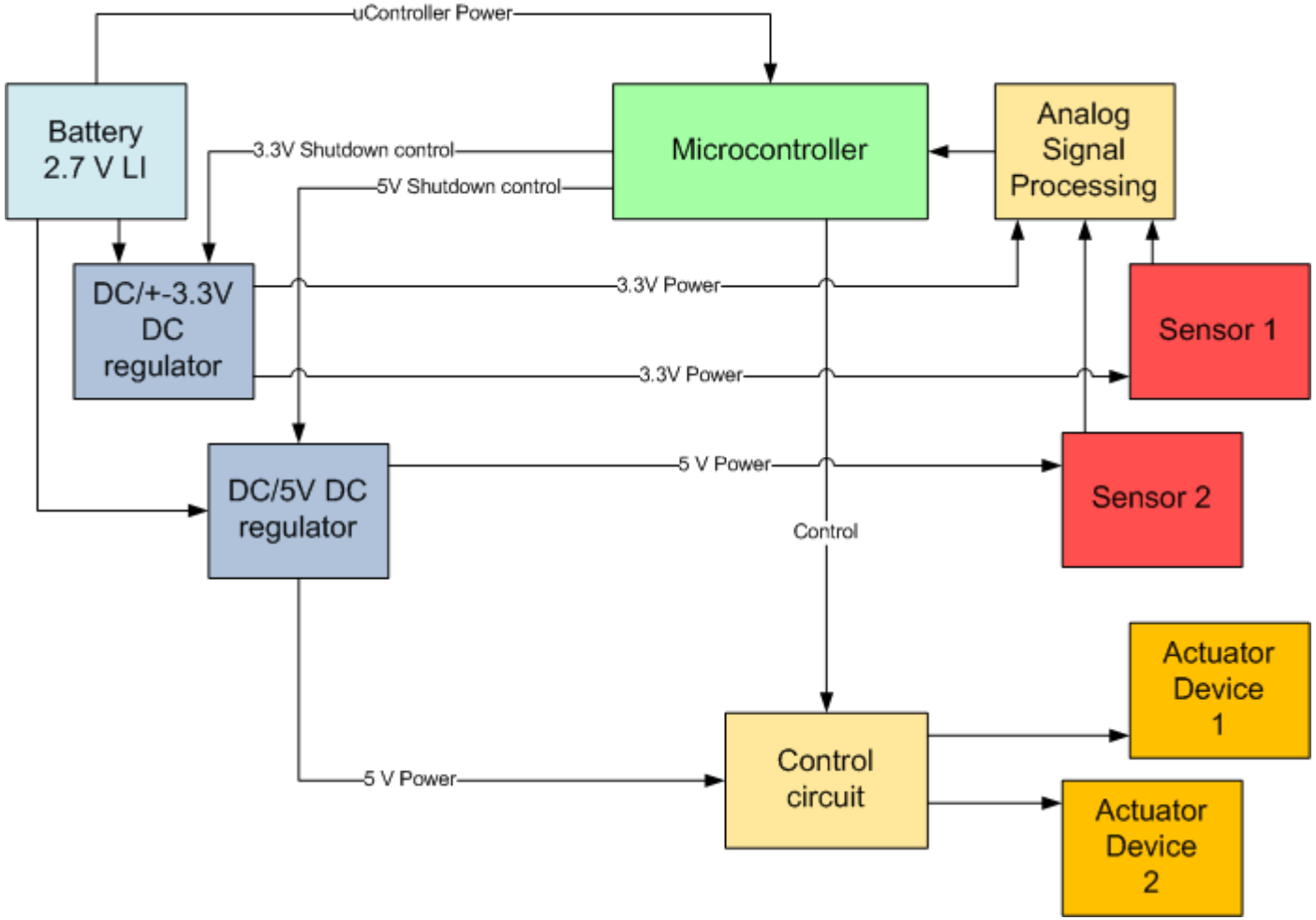
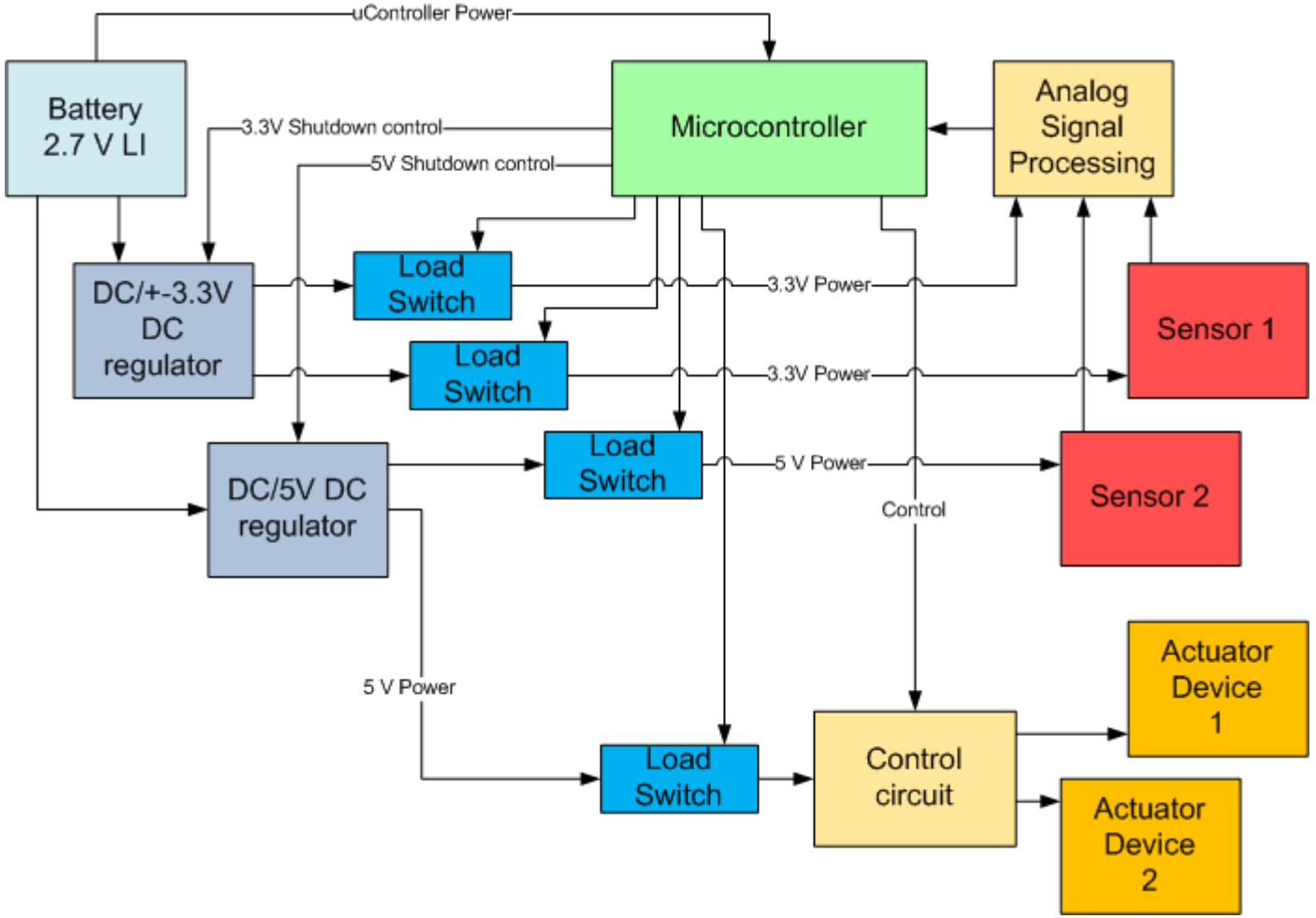
Load switching concept

- In low-power systems, leakages in peripherals are minimized by powering OFF to those peripherals
- Low-power MCU include internal methods for powering OFF internal peripherals
- Power control must be added for external peripherals
  - Methods:
    - Control of source devices (eg. DC/DC converters or regulators)
      - Increased component count -> increased board space and cost
    - Load switch
      - More flexible than enabling or disabling the power supply rails
      - May be redundant with source device control
    - Peripherals with built in load control
      - Lower component count
      - Part availability is less or non-existant

Power management via control of source devices



Power management via control of load switches

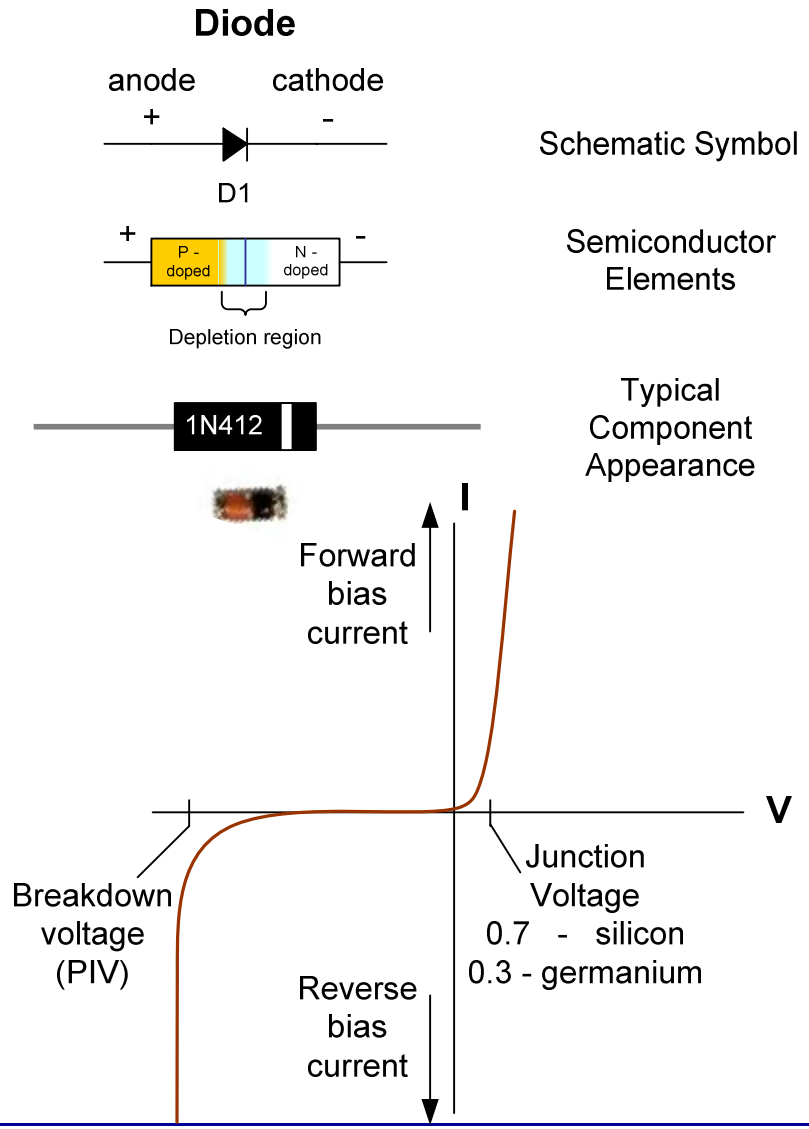


Load switch design issues

- Complicated because of many requirements:
  - Low quiescent and OFF leakage levels
    - Desirability of MOSFET solutions, but difficult gate voltages
  - Management of in-rush current when switched ON
  - Need for very low voltage drop across switch
    - Allow effective battery use
    - Minimize power losses in switching
  - Need to discharge circuit being powered OFF
- Approach here:
  - Review MOSFET application and load switch design

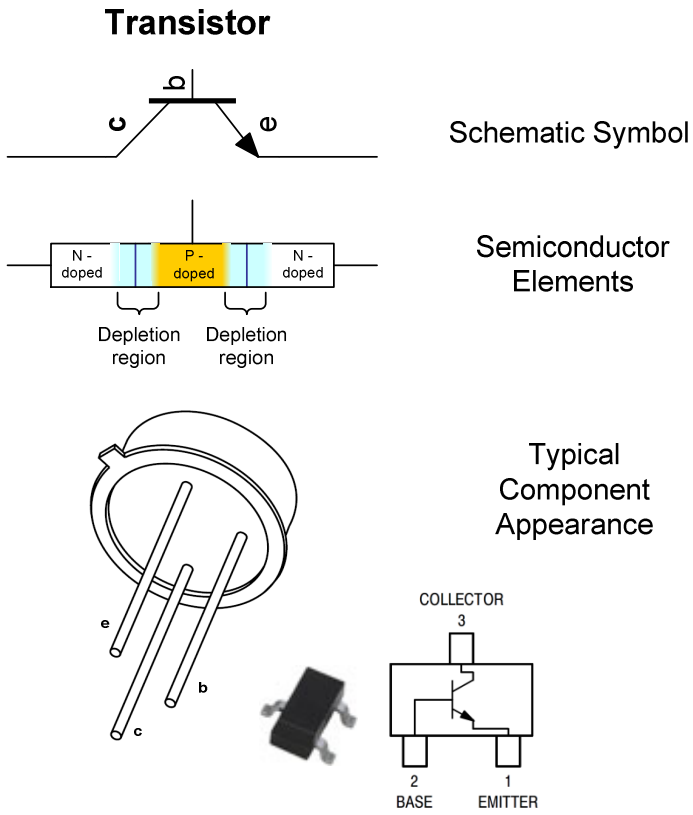
Semi-conductor review

- Check valve behavior
  - Diffusion at the PN junction of P into N and N into P causes a depleted non-conductive region
  - Depletion is enhanced by reverse bias
  - Depletion is broken down by forward bias
- When forward biased
  - High current flow junction voltage
- When reverse biased
  - Very low current flow unless above peak inverse voltage (PIV) (damaging to rectifying diodes, OK for zeners)



Transistor devices

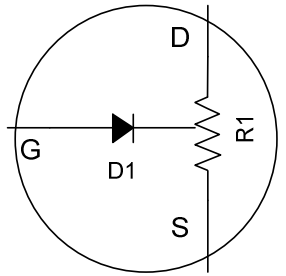
- Construction
  - Analogous to two diodes with a p-p (for an NPN device), or an n-n connection (for a PNP device)
  - Connections
    - Collector
    - Base
    - Emitter
- Nature of the device (NPN)
  - Reverse bias on the C-B junction and a moderate forward bias on the B-E junction causes current flow from C to E. Current is proportional to gain times B-E current in the linear range of the device
  - PNP requires reverse polarities and has reverse current flow.



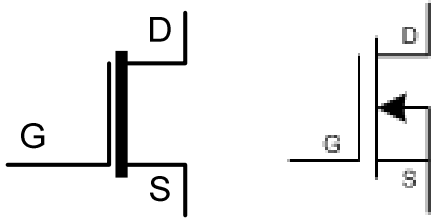
Junction Field Effect Transistors

- Transconductance is controlled by V_{GS}
- Pinched gate technology
- High gate impedance
- Heavily used for power drive circuits

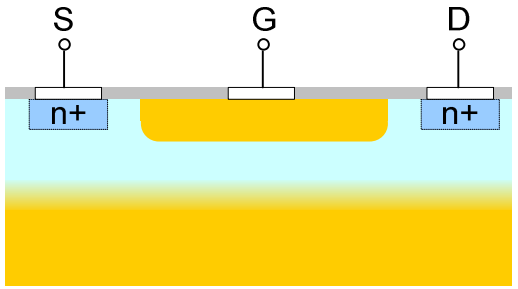
- Field Effect Functional Model
  - N Channel



- Schematic symbols

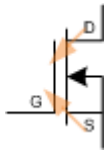


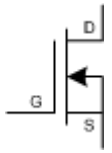
- Semiconductor elements



MOSFET Biasing

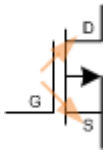
- Simplistic model
  - N Channel FET
    - $V_G - V_S > V_T$ (G – gate, S – source, T – Threshold)
    - $V_G - V_D > V_T$

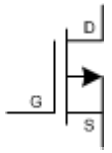




N MOSFET

  - P Channel FET
    - $V_S - V_G > V_T$
    - $V_D - V_G > V_T$



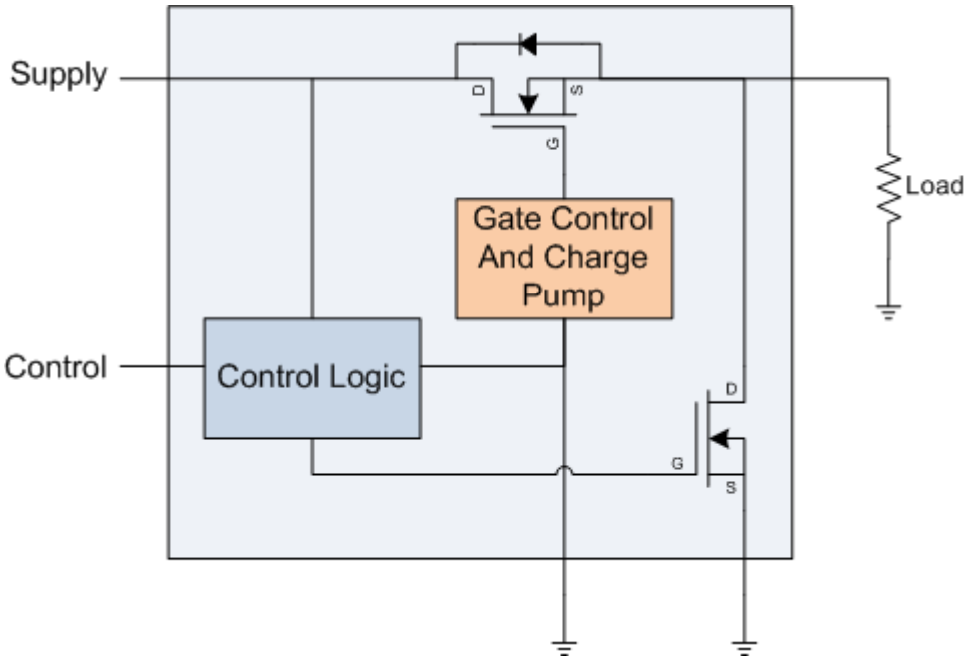


P MOSFET

  - Under these conditions, V_G controls I_{SD}
  - Gate voltage levels are problematic for single rail systems
    - Integrated solutions exist with built=in charge pump or level shift
    - Integrated solutions optimized for low-power designs

Integrated Load Switch

- High-side load switch made of three elements:
  - Pass element
    - Typically an enhancement-mode MOSFET.
  - Gate control and charge pump
    - Provides necessary switching voltage to the gate of the pass element
  - Input logic
    - Interprets control enable signal and triggers the gate control
  - In-rush control or rise time control may be included



Design parameters for integrated load switches

- Important Design Parameters:
  - R_{ON} – FET On-state resistance from drain to source
    - Controls voltage drop / power when ON
  - t_{RISE} – Rise time of the switch
    - In-rush current
  - V_{IH}/V_{IL} – Control thresholds of the switch
  - I_{CC} and $I_{SHUTDOWN}$ – Quiescent and shutdown current
  - Quick Output Discharge feature